Report of the activity of Leonel Sousa as Visiting Professor in

Electrical and Computer Engineering (ECE) Depart. at Carnegie Mellon University - CMU PT Program

I have stayed from the beginning of September to the end of November, uninterruptedly, in Pittsburgh, at CMU, hosted in the Computer Architecture Lab headed by Prof. James C. Hoe. During my stay, engaged in a lot of activities that not only enrich my scientific and technical knowledge but also expose me to the everyday academic life of one of the top Universities in the world.

I have made several presentations and I have given a tutorial based on my previous research work in Portugal at IST, both at the CMU and in conferences, namely:

- "CARM: Cache-aware Roofline model for Multicores", Computer Architecture Lab (CALCM) Seminars, CMU, Pittsburgh, September 27 (http://www.ece.cmu.edu/~calcm/doku.php?id=seminars:seminars)
- "Efficient HEVC Decoder for Heterogeneous CPU with GPU Systems", communication in the 2016 IEEE Workshop on Multimedia Signal Processing (MMSP 2016), Montreal, Canada, September 22 (http://mmsp2016.ece.mcgill.ca/Program/Program.htm)
- "Performance, Power and Energy-Efficiency Insightful Modeling of Multi-Cores", Tutorial, The 34th IEEE International Conference on Computer Design (IICD), Phoenix, US, October 2 (http://www.iccd-conf.com/Program_2016.html)

In what concerns research, I have carefully analysed the architecture and the technology of the most recent processing acceleration fabrics investigated in the scope of the *Catapult* Project, from Microsoft, and the *Hardware Accelerator Research* Program, from Intel. Regarding the *Catapult* Project, I have also followed the work of a Master Student, supervised by Prof. James C. Hoe, deploying simple FFT accelerators on the Microsoft Cluster hosted in UTAustin. Regarding the *Hardware Accelerator Research* Program, based on the knowledge acquired during my stay, I have submitted a proposal, titled "Exploring the efficiency limits of heterogeneous CPU+FPGA systems", which has successfully been accepted in the INTEL internal evaluation process and then a new research project will start, in the beginning of 2017, between IST and Intel.

In terms of teaching, I have not taught any classes, but I followed the F16 Master Course, Reconfigurable Logic: Technology, Architecture and Applications, taught by Prof. James Hoe. It has been quite interesting to have contact with the organization of the course and the interesting projects on HLS.

Moreover, I contacted several professors of the ECE Department of CMU, namely the Head of the Department Prof. Jelena Kovačević, and I attended a faculty meeting of the Department by invitation.

In conclusion, it was a quite valuable experience, for which I would like to thank the CMU-Portugal program support and the time and support of my host, Prof. James Hoe, which have provided me an unforgettable experience.